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Claims

[c1] 1.An integrated circuit comprising:
a bondable metal pad defined on a stress-buffering dielectric layer;
a damascened intermediate metal layer fabricated in a first inter-metal dielectric (IMD) layer that is under said stress-buffering dielectric layer, and said damascened intermediate metal layer being disposed directly under said bondable metal pad and electrically connected to said bondable metal pad through a plurality of via plugs integrated with said bondable metal pad;
at least one damascened metal frame fabricated in a second IMD layer under said first IMD layer, said damascened metal frame being disposed directly under said damascened intermediate metal layer; and
a portions of active circuit components of said integrated circuit disposed directly under said damascened metal frame.

[c2] 2.The integrated circuit according to claim 1 wherein said stress-buffering dielectric layer is structurally denser than any of said first IMD layer and second IMD layer.

[c3] 3.The integrated circuit according to claim 2 wherein said stress-buffering dielectric layer is made of silicon dioxide.

[c4] 4.The integrated circuit according to claim 1 wherein said stress-buffering dielectric layer and a peripheral area of said bondable metal pad is covered by a passivation layer.

[c5] 5.The integrated circuit according to claim 4 wherein said passivation layer is made of silicon nitride.

[c6] 6.The integrated circuit according to claim 4 wherein said passivation layer is made of polyimide.

[c7] 7.The integrated circuit according to claim 4 wherein said passivation layer has a window exposing a top surface area of said bondable metal pad.

[c8] 8.The integrated circuit according to claim 1 wherein said damascened intermediate metal layer comprises copper conductor core and a diffusion barrier layer disposed between said copper conductor core and said first IMD layer.

[c9] 9.The integrated circuit according to claim 1 wherein said bondable metal pad comprises aluminum.

[c10] 10.The integrated circuit according to claim 1 wherein said plural via plugs are made of aluminum.

[c11] 11.The integrated circuit according to claim 1 wherein said damascened metal frame comprises copper.

[c12] 12.An integrated circuit comprising:
an aluminum bonding pad defined on a stress-buffering dielectric layer;
an aluminum active circuit layout, wherein said aluminum active circuit layout and said aluminum bonding pad are simultaneously defined on said stress-buffering dielectric layer;
a damascened intermediate copper layer fabricated in a first inter-metal dielectric (IMD) layer that is under said stress-buffering dielectric layer, and said damascened intermediate copper layer being disposed directly under said aluminum bonding pad and electrically connected to said aluminum bonding pad through a plurality of via plugs integrated with said aluminum bonding pad;
at least one damascened copper frame fabricated in a second IMD layer under said first IMD layer, said damascened copper frame being disposed directly under said damascened intermediate copper layer; and
a portions of active circuit components of said integrated circuit disposed directly under said damascened metal frame.

[c13] 13.The integrated circuit according to claim 12 wherein said stress-buffering dielectric layer is structurally denser than any of said first IMD layer and second IMD layer.

[c14] 14.The integrated circuit according to claim 13 wherein said stress-buffering dielectric layer is made of silicon dioxide.

[c15] 15.The integrated circuit according to claim 12 wherein said stress-buffering dielectric layer, said aluminum active circuit layout over said stress-buffering dielectric layer, and a peripheral portions of said aluminum bonding pad are covered by a passivation layer.

[c16] 16.The integrated circuit according to claim 15 wherein said passivaiton layer is made of polyimide.